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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,677	02/01/2002	Robert J. Devins	BUR920010098	3095

30449 7590 10/26/2005

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,677	DEVINS ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been presented for examination based on the application filed on 1 February 2002.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steinmetz, Jr. "Hardware Simulation and Design Verification System and Method" U.S. Patent No. 5,600,579**,

hereafter referred to as **"Steinmetz"** in view of **Lee et al. "Semiconductor Integrated Device" U.S. Patent No. 5,805,605** hereafter referred to as **"Lee"**.

Regarding Claims 1, 8, and 15:

Steinmetz discloses a system, method, and program storage device for verifying an integrated circuit design: **(Steinmetz. Column 2, Lines 66-67. Column 5, Lines 1-19)**

as well as a test operating system **(Steinmetz. Column 5, Lines 37-46)**

Steinmetz does not disclose the integrated circuit comprising

an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design; an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models; a bus for transferring signals between said I/O controller and said switch;

Lee, however, discloses the integrated circuit comprising

an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design; **(Lee. Column 4, Lines 1-11. Figure 4, Elements 2,4, 10, and 12)**

an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models; **(Lee. Column 4, Lines 12-22. Figure 4, Elements 1a-1d, 6, 8, and 16)**

a bus for transferring signals between said I/O controller and said switch; **(Lee. Column 4, Lines 7-11. Figure 4, Elements N1-N5)**

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the semiconductor integrated device capable of selective execution as discussed in **Lee**, and to further provide a verification of the design utilizing a controlling test as discussed in **Steinmetz** in order to allow for reduced verification time.

Regarding Claim 2, 9, and 16:

Steinmetz does not disclose the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models.

Lee, however, discloses the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models. **(Lee. Column 4, Lines 1-22. Figure 4)**

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the semiconductor integrated device as discussed in **Lee**, and to further provide a verification of the design as discussed in **Steinmetz** in order to allow for reduced verification time.

Regarding Claim 3, 10, and 17:

Steinmetz discloses the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device further includes an address register. **(Steinmetz. Column 6, Lines 40-44)**

Steinmetz does not disclose the address register for setting said switch and controlling said I/O driver models.

Lee, however, discloses the address register for setting said switch and controlling said I/O driver models. **(Lee. Column 4, Lines 1-22. Figure 4)**

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize an address as discussed in **Steinmetz** in order to set the switch and control the I/O driver as disclosed in **Lee**, in order to allow for proper memory location allocation.

Regarding Claim 4, 11, and 18:

Steinmetz discloses The system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said integrated circuit design further includes an embedded processor for running

said test operating system. **(Steinmetz. Column 5, Lines 15-20, 37-46. Figure 1. Element 103, 115, 113, 107 and 101.)**

Regarding Claim 5, 12 and 19:

Steinmetz discloses the system, method, and program storage device of claims 2, 9, and 16 respectively, wherein each said external memory mapped test device module further includes an address register. **(Steinmetz. Column 6, Lines 40-44)**

Steinmetz does not disclose the address register for setting said portion of said switch and controlling said one I/O driver model.

Lee, however, discloses the address register for setting said portion of said switch and controlling said one I/O driver model. **(Lee. Column 4, Lines 1-22. Figure 4)**

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize an address as discussed in **Steinmetz** in order to set the switch and control the I/O driver as disclosed in **Lee**, in order to allow for proper memory location allocation.

Regarding Claim 6, 13, and 20:

Steinmetz discloses The system, method, and program storage device of claims 2, 9, and 16 respectively, wherein said integrated circuit design further includes an embedded processor for running said test operating system. **(Steinmetz. Column 5, Lines 15-20, 37-46. Figure 1. Element 103, 115, 113, 107 and 101.)**

Regarding Claim 7:

Steinmetz does not disclose the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each

additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design.

Lee, however, discloses the system, method, and program storage device of claims 1, 8, and 15 respectively, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design. **(Lee. Column 4, Lines 1-22. Figure 4)**

It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the semiconductor integrated device as discussed in **Lee**, and to further provide a verification of the design as discussed in **Steinmetz** in order to allow for reduced verification time.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references include:

A) "System and Method Relating to Verification of Integrated Circuit Design" Meiyappan et al. WO0201424.

B) 'A la Carte, SOC's require innovative IO management. David Murray, Michael Phelan, Duolog Technologies.

C) Synplicity, Cerifty Software.

D) "Method and Apparatus for Design Verification of an Integrated Circuit Using a Simulation Test Bench Environment" Reise. U.S. Patent No. 6,498,999.

4. All Claims are rejected.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA
September 16, 2005

JEAN R. HOMERE
PRIMARY EXAMINER